CLAIMS

1. A method for computing a level-of detail (LOD) for application of texels of a texture map to pixels of a graphics image, the method comprising:

calculating the square of the ratio between the number of texels for one pixel;

approximating a base-two logarithm of the square of the ratio; and

dividing the result by two to provide the LOD.

2. The method of claim 1 wherein dividing the result by two comprises shifting a binary value of the LOD right one-bit.

3. The method of claim 1 wherein calculating the square of the ratio comprises:

calculating the square of a first ratio between the number of texels for one pixel along a first axis and the square of a second ratio between the number of texels for one pixel along a second axis orthogonal to the first axis; and

selecting the greater of the square of the first ratio and the square of the second ratio for calculating the LOD.

4. The method of claim 1 wherein the square of the ratio comprises an unsigned fixed-point binary value having a number of integer bits and fractional bits, and approximating a base-two logarithm of the square of the ratio comprises:

shifting the square of the ratio left by the number of leading zeros (LZs) and ignoring the most significant bit (MSB) of the resulting number to produce a first number;

calculating a six-bit signed integer value from the equation:

```
6-bit signed integer=[(number of integer bits-1)-LZs];
```

concatenating the six-bit signed integer value to the first number; and

defining the five MSBs of the resulting number as the signed integer portion of the LOD.

5. The method of claim 1 wherein the square of the ratio comprises an unsigned fixed-point binary value having an integer portion and a fractional portion.

6. The method of claim 5 wherein the integer portion is 27 bits in length.

7. The method of claim 5 wherein the fractional portion is 5 bits in length.

8. The method of claim 1 wherein the LOD comprises a signed fixed point binary value having an integer portion and a fractional portion.

9. The method of claim 8 wherein the integer portion is five bits in length.

10. A method for computing a level-of detail (LOD) for application of texels of a texture map to pixels of a graphics image, the method comprising:

calculating the square of a first ratio between the number of texels for one pixel along a first axis and the square of a second ratio between the number of texels for one pixel along a second axis orthogonal to the first axis;

selecting the greater of the square of the first ratio and the square of the second ratio for calculating the LOD;

shifting the selected square of the ratio left by the number of leading zeros (LZs) and ignoring the most significant bit (MSB) of the resulting number to produce a first number;

calculating a six-bit signed integer value from the equation:

```
6-bit signed integer=[(number of integer bits -1)-LZs],
```

where `number of integer bits` is the number of integer bits representing the selected square of the ratio;

concatenating the six-bit signed integer value to the first number;

defining the five MSBs of the resulting number as a signed integer portion; and

shifting the resulting binary number right by one-bit to provide the LOD.

11. The method of claim 10 wherein the square of the ratio comprises an unsigned fixed-point binary value having an integer portion and a fractional portion.

12. The method of claim 11 wherein the integer portion is 27 bits in length.

13. The method of claim 11 wherein the fractional portion is 5 bits in length.

14. The method of claim 10 wherein the LOD comprises a signed fixed point binary value having an integer portion and a fractional portion.

15. The method of claim 14 wherein the integer portion is five bits in length.

16. An apparatus adapted to receive signals representing texel coordinates for texels of a texture map and pixel coordinates for pixels of a graphics image to calculate a level-of-detail (LOD), the apparatus calculating the square of the ratio between the number of texels applied to one pixel from the texel and pixel coordinates, approximating a base-two logarithm of the square of the ratio, and dividing the result of the approximation by two to compute the LOD.

17. The apparatus of claim 16 having a shifting circuit coupled to receive the result of the approximation and adapted to divide the approximation by two by shifting the approximation right one-bit.

18. The apparatus of claim 16 wherein calculating the square of the ratio comprises:

calculating the square of a first ratio between the number of texels for one pixel along a first axis and the square of a second ratio between the number of texels for one pixel along a second axis orthogonal to the first axis; and

selecting the greater of the square of the first ratio and the square of the second ratio for calculating the LOD.

19. The apparatus of claim 16 wherein the square of the ratio comprises an unsigned fixed-point binary value having a number of integer bits and fractional bits, and approximating a base-two logarithm of the square of the ratio comprises:

shifting the square of the ratio left by the number of leading zeros (LZs) and ignoring the most significant bit (MSB) of the resulting number to produce a first number;

calculating a six-bit signed integer value from the equation:

```
6-bit signed integer=[(number of integer bits-1)-LZs];
```

concatenating the six-bit signed integer value to the first number; and

defining the five MSBs of the resulting number as the signed integer portion of the LOD.

20. The apparatus of claim 16 wherein the square of the ratio comprises an unsigned fixed-point binary value having an integer portion and a fractional portion.

21. The apparatus of claim 20 wherein the integer portion is represented by 27 bits.

22. The apparatus of claim 20 wherein the fractional portion is represented by 5 bits.

23. The apparatus of claim 1 wherein the LOD comprises a signed fixed point binary value having an integer portion and a fractional portion.

24. The apparatus of claim 8 wherein the integer portion is represented by five bits.

25. An apparatus for computing a level-of-detail (LOD) for application of texels of a texture map to pixels of a graphics image, the apparatus comprising:

a means for calculating the square of the ratio between the number of texels applied to one pixel from the texel coordinates of a texture map and pixel coordinates for pixels of a graphics image;

a means for approximating a base-two logarithm of the square of the ratio; and

a means for dividing the result of the approximation by two to compute the LOD.

26. A graphics processing system, comprising:

a bus interface for coupling to a system bus;

a graphics processor coupled to the bus interface to process graphics data;

address and data busses coupled to the graphics processor to transfer address and graphics data to and from the graphics processor;

display logic coupled to the data bus to drive a display; and

a LOD computation circuit coupled to the graphics processor adapted to receive signals representing texel coordinates for texels of a texture map and pixel coordinates for pixels of a graphics image to calculate a level-of-detail (LOD), the computation circuit calculating the square of the ratio between the number of texels applied to one pixel from the texel and pixel coordinates, approximating a base-two logarithm of the square of the ratio, and dividing the result of the approximation by two to compute the LOD.

27. The graphics processing system of claim 26 wherein the LOD computation circuit comprises a shifting circuit coupled to receive the result of the approximation and adapted to divide the approximation by two by shifting the approximation right one-bit.

28. The graphics processing system of claim 26 wherein calculating the square of the ratio by the LOD computation circuit comprises:

calculating the square of a first ratio between the number of texels for one pixel along a first axis and the square of a second ratio between the number of texels for one pixel along a second axis orthogonal to the first axis; and

selecting the greater of the square of the first ratio and the square of the second ratio for calculating the LOD.

29. The graphics processing system of claim 26 wherein the square of the ratio calculated by the LOD computation circuit comprises an unsigned fixed-point binary value having a number of integer bits and fractional bits, and approximating a base-two logarithm of the square of the ratio by the LOD computation circuit comprises:

shifting the square of the ratio left by the number of leading zeros (LZs) and ignoring the most significant bit (MSB) of the resulting number to produce a first number;

calculating a six-bit signed integer value from the equation:

```
6-bit signed integer=[(number of integer bits-1)-LZs];
```

concatenating the six-bit signed integer value to the first number; and

defining the five MSBs of the resulting number as the signed integer portion of the LOD.

30. The graphics processing system of claim 26 wherein the square of the ratio calculated by the LOD computation circuit comprises an unsigned fixed-point binary value having an integer portion and a fractional portion.

31. The graphics processing system of claim 30 wherein the integer portion of the square of the ratio is represented by 27 bits.

32. The graphics processing system of claim 30 wherein the fractional portion of the square of the ratio is represented by 5 bits.

33. The graphics processing system of claim 26 wherein the LOD computed by the LOD computation circuit comprises a signed fixed point binary value having an integer portion and a fractional portion.

34. The graphics processing system of claim 33 wherein the integer portion of the LOD computed by the LOD computation circuit is represented by five bits.

35. A computer system, comprising:

a system processor;

a system bus coupled to the system processor;

a system memory coupled to the system bus; and

a graphics processing system coupled to the system bus, the graphics processing system, comprising:

a bus interface for coupling to a system bus;

a graphics processor coupled to the bus interface to process graphics data;

address and data busses coupled to the graphics processor to transfer address and graphics data to and from the graphics processor;

display logic coupled to the data bus to drive a display; and

a LOD computation circuit coupled to the graphics processor adapted to receive signals representing texel coordinates for texels of a texture map and pixel coordinates for pixels of a graphics image to calculate a level-of-detail (LOD), the computation circuit calculating the square of the ratio between the number of texels applied to one pixel from the texel and pixel coordinates, approximating a base-two logarithm of the square of the ratio, and dividing the result of the approximation by two to compute the LOD.

36. The computer system of claim 35 wherein the LOD computation circuit comprises a shifting circuit coupled to receive the result of the approximation and adapted to divide the approximation by two by shifting the approximation right one-bit.

37. The computer system of claim 35 wherein calculating the square of the ratio by the LOD computation circuit comprises:

calculating the square of a first ratio between the number of texels for one pixel along a first axis and the square of a second ratio between the number of texels for one pixel along a second axis orthogonal to the first axis; and

selecting the greater of the square of the first ratio and the square of the second ratio for calculating the LOD.

38. The computer system of claim 35 wherein the square of the ratio calculated by the LOD computation circuit comprises an unsigned fixed-point binary value having a number of integer bits and fractional bits, and approximating a base-two logarithm of the square of the ratio by the LOD computation circuit comprises:

shifting the square of the ratio left by the number of leading zeros (LZs) and ignoring the most significant bit (MSB) of the resulting number to produce a first number;

calculating a six-bit signed integer value from the equation:

```
6-bit signed integer=[(number of integer bits-1)-LZs];
```

concatenating the six-bit signed integer value to the first number; and

defining the five MSBs of the resulting number as the signed integer portion of the LOD.

39. The computer system of claim 35 wherein the square of the ratio calculated by the LOD computation circuit comprises an unsigned fixed-point binary value having an integer portion and a fractional portion.

40. The computer system of claim 39 wherein the integer portion of the square of the ratio calculated by the LOD computation circuit is represented by 27 bits.

41. The computer system of claim 39 wherein the fractional portion of the square of the ratio calculated by the LOD computation circuit is represented by 5 bits.

42. The computer system of claim 35 wherein the LOD computed by the LOD computation circuit comprises a signed fixed point binary value having an integer portion and a fractional portion.

43. The computer system of claim 42 wherein the integer portion of the LOD computed by the LOD computation circuit is represented by five bits.